

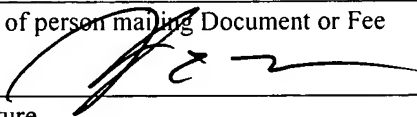
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited  
with the United States Postal Service with sufficient postage  
as first class mail in an envelope addressed to: Mail Stop  
Amendment, Commissioner for Patents, P.O. Box 1450,  
Alexandria, VA 22313-1450 on February 3, 2005  
(Date of Deposit)

Harold C. Moore

Name of person mailing Document or Fee

  
Signature

February 3, 2005

Date of Signature

Re:	Application of:	Kahlisch et al.
	Serial No.:	10/719,999
	Filed:	November 21, 2003
	For:	Supporting Structure for a Chip and Method for Producing the Same
	Group Art Unit:	2814
	Confirmation No.:	1506
	Examiner:	Shrinivas H. Rao
	Our Docket No.:	1890-0011

**TRANSMITTAL OF RESPONSE TO OFFICE ACTION**

Please find for filing in connection with the above patent application the  
following:

1. Response to Office Action; and
2. One (1) return post card.

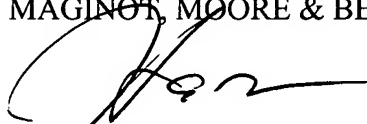
\* The fee has been calculated as shown below.

CLAIMS AS AMENDED				
	Claims Remaining After Amendment	Highest No. Paid For	Fee Calculation	Addit Fee
Total Claims	13	22	0 X 50	\$ 0.00
Independent Claims	1	2	0 X 200	\$ 0.00
Total Additional Fee Required				\$ 0.00

Please charge any fee deficiency, or credit any overpayment, to Deposit Account No. 13-0014; but not to include any payment of issue fees.

Respectfully Submitted,

MAGINOT, MOORE & BECK



February 3, 2005

Harold C. Moore  
Registration No. 37,892  
Bank One Center/Tower  
111 Monument Circle, Suite 3000  
Indianapolis, Indiana 46204-5115

Enclosures

IFW

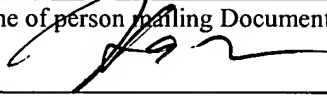


IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Mail Stop Amendment  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on February 3, 2005  
(Date of Deposit)

Harold C. Moore  
Name of person mailing Document or Fee

  
Signature

February 3, 2005  
Date of Signature

Re:    Application of:        Kahlisch et al.  
      Serial No.:            10/719,999  
      Filed:                November 21, 2003  
      For:                  Supporting Structure for a Chip and Method  
                                  for Producing the Same  
      Group Art Unit:        2814  
      Confirmation No.:     1506  
      Examiner:             Shrinivas H. Rao  
      Our Docket No.:       1890-0011

RESPONSE TO OFFICE ACTION

Sir:

In response to the Office Action dated December 3, 2004 for the above-identified patent application, please amend the application as follows:

- Amendments to the Disclosure begin on page 2 of this document.
- Amendments to the Claims begin on page 4 of this document.

Amendments to the Disclosure

Please replace the paragraph that begins on page 1, line 20 with the following amended paragraph:

In the production of miniature packages, a specially preprocessed support substrate is typically used in the prior art. Here, both a voltage-absorbing bilaterally adhesive elastomer and a printed adhesive layer are disposed on the supporting substrate, so that a so-called bonding channel is recessed in an end-to-end manner by division. The bonding channel enables the electrical connection of pads that are disposed on a chip, wherein the chip is attached to the support substrate. In particular, the pads are connected by~~electrically connecting pads on a chip, which is attached on the supporting substrate, by means of~~wires that are passed through the bonding channel for example to terminal regions of the supporting substrate.

Please replace the paragraph that begins on page 1, line 32, with the following amended paragraph:

Typically, the wire bonding takes place after connecting the chip with the supporting substrate. Here, the wires are inserted from outside into the bonding channel by means of known methods ~~from outside~~ via bond openings, and then are in order to then being connected to the pads on the chip. The bonding channel typically has a width of about 0.7 to 1.2 mm, wherein the length thereof may extend across the entire supporting substrate. Thereby, ~~by means of~~a single channel may provide, an electrical connection for a plurality of pads of the chip ~~may be provided~~.

Please replace the paragraph that begins on page 4, line 21, with the following amended paragraph:

It is the aim of ~~In one embodiment~~ to reduce the capillary effect occurring at the

~~escape prevention structure to avoid escape, for avoiding leaving~~ of the encapsulation mass, ~~it is being aimed at reducing the capillary effect occurring at the escape prevention structure, such that the pulling out of the encapsulating mass through the escape prevention structure due to occurring capillary forces is prevented.~~ For example, in one embodiment, an escape of the encapsulation mass occurring in the prior art in bonding channels with laterally open ends due to capillary forces may be achieved by narrowing the bonding channel cross-section at the ends ~~by means of~~ using barrier structures.

Please replace the paragraph that begins on page 7, line 11, with the following amended paragraph:

In a further embodiment, ~~in which~~ a recess for venting is formed in the region of the bonding channel on the supporting substrate, ~~the~~ The recess extends in a direction perpendicular to the supporting substrate from the surface of the supporting substrate on which the interconnect layer is formed to the opposing surface.

Please replace the paragraph that begins on page 9, line 24, with the following amended paragraph:

Fig. 1a shows a schematically illustrated cross-section through a supporting structure with an applied chip according to an embodiment of the present invention. An interconnect layer 110 with a bonding channel 114 formed therein is disposed on a surface 100a of the supporting substrate 100. ~~By a A bonding channel, a recess is to be understood to be a recess is able that enables to pass wires from a pad of a chip 112 applied on an outer surface 100a-110a of the interconnect layer 110 to the surface 100a of the supporting substrate 100 opposing the chip 112. According to Fig. 1b, which shows showing a plan view onto of the supporting structure without the chip 112, the bonding channel 114 is formed by a division of the interconnect layer 100. In other words, the bonding channel 114 is formed by a horizontally extending elongated recess in the interconnect layer 110, with it being open at lateral ends 114a and 114b.~~